Design and Analysis of a Multi-Layer Transformer Balun for Silicon RF Integrated Circuits

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Abstract **In this paper, we present the design and analysis of an on-chip transformer balun for silicon RFIC. Both the primary and secondary spread over four metal layers along a common symmetric axis to reduce the overall area maintaining reasonable quality factor. A five-port transformer balun circuit model is developed to facilitate the device simulation. A 4:11 transformer balun is fabricated and test. It is ideal for LNA to enhance the gain with optimum noise figure.**

I. Introduction

Transformers can provide amplification of current or voltage swings as well as impedance matching from one circuit stage to another. In RFIC designs, transformer balun is also useful for conversion between differential and single-end signals. It is desirable to place RFIC transformer baluns on chip to reduce the cost of on-board off-chip components. Recently, there have been many prior attempts to integrate transformer and/or baluns on-chip in RFIC [1-5]. Prior work on on-chip transformers is best summarized in Reference [4]. Various transformer layouts including parallel winding, inter-wound winding, overlay winding, and concentric spiral winding were discussed. Several factors limit the application of on-chip transformers in RFIC. First, the magnetic core that is commonly used in electric circuits to confine magnetic flux is not applicable. As a result, the flux leakage and capacitive coupling degrade the transformer performance. Second, the series resistance associated with the metal windings is often significant due to the fact that the metal thickness is usually much less than its skin depth in present silicon IC process. The resulting current consumption and power loss at the transformer are usually much higher than what is desirable. In this paper, we propose a transformer/balun structure that provides better quality factor (lower loss) with smaller size as compared with other similar on-chip balun layouts for thin metal layer RFIC. An example of the layout of this 4-metal layer transformer balun is shown in Figure 1.

II. Design, Simulation, and Models

The proposed transformer is particularly suitable for multi-layer structures where the metal layers spread over several surfaces. It is known that for an on-chip inductor, all the metal windings on the same surface would usually result in lower quality factor (Q) and larger dimensions than the case when the metal windings spread over multiple layer surfaces due to flux cancellation and eddy current effects.

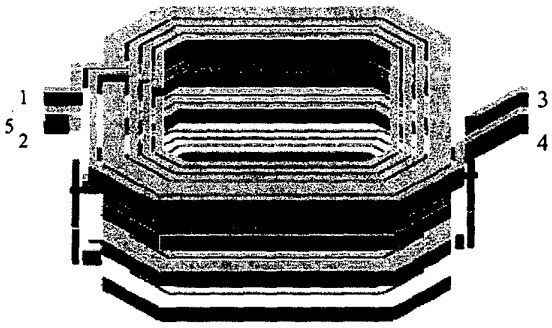

Figure 1. A toroidal and concentric transformer balun.

Figure 1 shows an example of the design. The primary (with wider tracks) with terminal ports 1 and 2 comprises the outer turns spread over four metal layers connected through vias. Secondary (with thinner track) comprises the inner turns also spread over four layers. Ports 3 and 4 are the differential ports and port 5 is the center-tap port. Ports 3, 4 and 5 are all in the secondary. Primary has a total of 4 turns (1-1-1-1 in four layers) and secondary has a total of 11 turns (3-2-2-4 in the four layers). The metal layers are wound in an octagon shape to reduce the overall metal strip length and thus the line resistance. The primary and secondary only are shown in Figures 2 and 3, respectively.

Figure 2. The primary of the toroidal transformer balun. Note the via for interconnection between metal layers.

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Figure 3. The secondary of the toridal transformer balun.

In order to have differential ports (output) on one side and the input port and ground ports on the other side, extra strip length in secondary is used to rout the ports to the desired locations.

The design of an on-chip transformer balun depends on specific applications. For example, the balun for LNA is to generate differential signals to the LNA from signal at antenna in a receiver mode. The load looking into LNA determines the overall size and turn ratio so that the on-chip impedance matching is applicable, the gain is maximized, and the noise figure is at an acceptable level. Note that for the balun under consideration, the primary and secondary currents are in opposite directions. The inductance of the primary, not the resistance is reduced or sometimes dictated by the induced flux in the secondary.

The secondary loading will usually reduce the primary Q and inductance while increases the capacitance. The reduction of the balun size will help increase the inductance. A design example is given here for 4 metal layer CMOS technology. The top metal thickness is 0.925μm and the remaining three metal layers are 0.64μm thick. The Silicon dioxide layers between metal layers are 1μm thick with a dielectric constant around 4.

Since high impedance load at the differential ports is usually the case, Q of the primary dictates the power loss and noise figure at the balun. In order to obtain a differential output, a center-tap ground is placed roughly midway through the secondary windings. The precise location can only be determined by several trial and errors in simulation.

Currently, there are many commercially available simulators for the design of RFIC inductors or transformers. Among them, IE3D integral-equation based full-wave simulator seems to be most suitable since it accurately takes into account the metal layer thickness and uses corrected surface-impedance model. A drawback is that it is intended for full-wave simulation and often takes excessive simulation time than necessary.

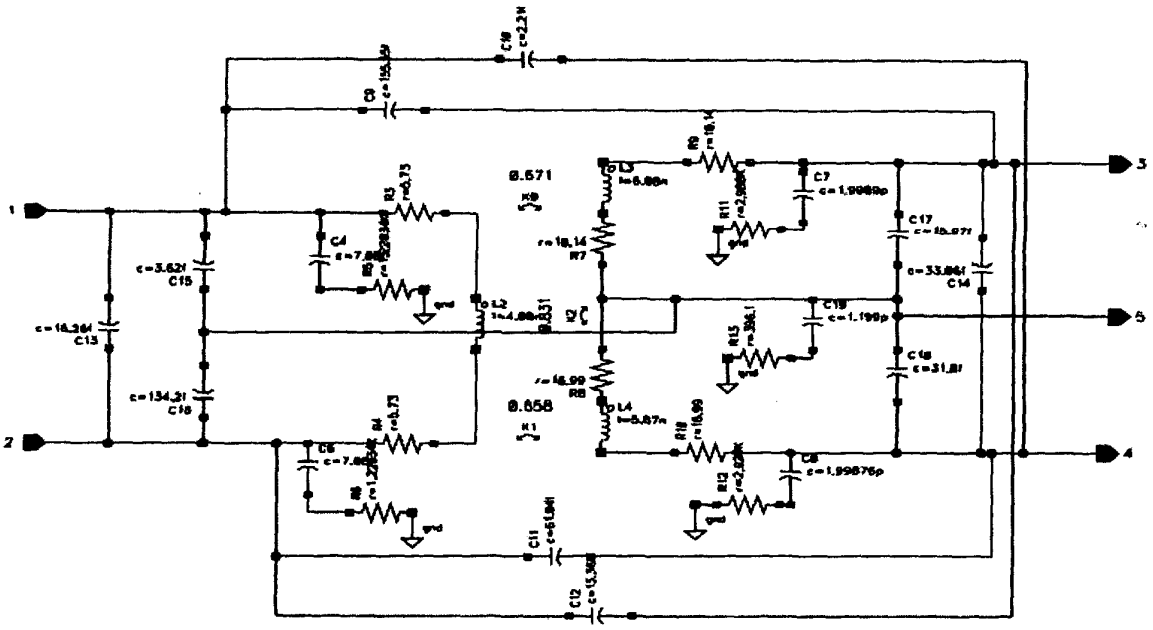

Figure 4. Five-port transformer balun circuit model.

The results of the full-wave simulation are five-port scattering parameters that can be easily converted into a Z or Y matrix and can be used directly for the design if the loading conditions are known. However, in order to combine the simulation with other active components such as LNA or PA, it is usually necessary to convert the scattering parameters to a circuit model for spice simulation. An example of the circuit model for the balun shown in Figure 1 is given in Figure 4.

In the transformer circuit model, port 1 and 2 denotes the two primary ports, typically one is an input/output port, and the other is ground. Port 3 and 4 are the two differential secondary output, with port 5 being the center tap point.

The main part of the transformer model is three coupled inductors L2, L3, and L4 consisted of the metal windings between Ports 1 and 2 (primary windings), between ports 3 and 5, and between ports 4 and 5, respectively. The center-tap ground basically divides the secondary into two inductors. k0, k1, and k2 represent the coupling coefficients between those inductors. The rest components are parasitic elements, including winding resistances, capacitances, and the substrate capacitances and losses. The S-parameters of the circuit model is fitted to those from the simulated or measured data, using commercially available optimization software tools. Either narrowband or broadband model can be obtained depending on the applications. The five-port scattering parameters usually agree within a few percentages between the full-wave simulation and the circuit model simulation. The circuit model also provides useful insight of the devices such as the substrate coupling, capacitive coupling between metal windings, inductive coupling efficiency, and various loss mechanisms.

III. Results and Discussion

The design example is intended for LNA that has an impedance of 70 Ω in series with a 146fF capacitor at around 2.4 GHz. The overall dimension is 135μmx135μm so that proper front end matching would result in high gain at the balun. The tuning circuit plus the voltage gain due to turn ratio provides about 13dB balun gain. High gain in balun is needed to reduce the noise figure and increase LNA sensitivity. The structure shown in Figure 1 is fabricated and test. The balun is used as a three-port circuit with one of the primary ports and the center-tap port grounded. The center-tap location is approximately half way of the secondary (the middle of the metal windings in the third layer counted from the top). The three-port schematics with new port definition are shown in Figure 5. Since only two-port measurement is available for us, three identical baluns are fabricated, each with one of the three different ports open-circuited.

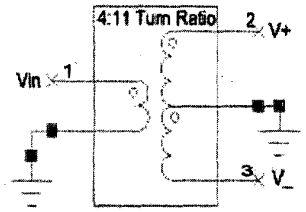

Figure 5. Three-port schematics of the transfomer balun.

The three-port Z matrix is constructed by the three measured two-port Z-matrices. In order to check the differential port amplitude and phase balance, Vin in Figure 5 is set to one and the differential open-circuit voltages at the secondary are obtained from both the simulated or measured three-port impedance matrix. The results are given in Table I. It is seen that simulation agrees very well with the measurement. The differential phase is about 5~6 degrees more than what is desired. The original design gives about 1 degree phase imbalance. The extra routing of the secondary winding to place the differential ports in close proximity degrades somewhat the phase balance. It is also seen that the voltage ratio is about 1.8 rather than 2.75 (11/4). This is due to the fact that concentric balun has a low coupling coefficient (about 0.65). The turn ratio provides about 5dB gain while the front tuning provides about 8 dB gain. The overall noise figure is calculated as about 3.7dB. The results of the amplitude balance check are further shown in Figure 6 with frequencies expanded from 0 to 6 GHz. It is seemed that the amplitude is very balanced over a broad frequency range. The voltage gain increases with frequencies till the balun resonant frequency is reached implying that the voltage gain is due to both inductive and capacitive coupling. Maximum coupling occurs near the resonant frequency of the primary (secondary is open-circuit here).

Table I. Differential Port Amplitude and Phase Balance Check.

Frequency (GHz)	Sim. $\|V_+\|$	Meas. $\|V_+\|$	Sim. $\|V_-\|$	Meas. $\|V_-\|$	Sim. $\angle V_+ - \angle V_-$	Meas. $\angle V_+ - \angle V_-$
2.40	0.889	0.904	0.891	0.913	185.1	186.0
2.43	0.894	0.910	0.896	0.921	185.2	185.9
2.46	0.898	0.919	0.898	0.923	185.3	186.0

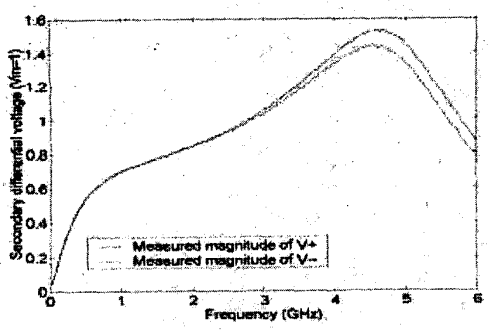

Figure 6. Measured magnitude of the differential open-circuit voltage when the primary voltage is 1

Practically, the quantity of most interest is the voltage gain at the LNA input or the current at the transmitting antenna for PA. For PA, there is a 3dB conjugate matching loss anyway. Power loss in balun is not the main issue. Nevertheless it provides useful insight of the balun circuit. Since the LNA is usually high impedance, most of the power consumption is expected to be in the primary. The return and insertion losses of the designed balun are calculated and the results are shown in Figure 7. In computation, the balun differential ports are loaded with 70 Ω in series with a 146fF capacitor to simulate the actual LNA input impedance. Tuning capacitor is in front of the balun to provide matching at around 2.4 GHz. The results of the S11 (return loss) and S12 and S13 (insertion loss) are shown in Figure 7. The curves for S12 and S13 are quite close, an indication of the amplitude balance of the differential ports. Within the operation band (around 2.4 GHz), the insertion loss for each differential port is about 10dB. This result indicates that there is about 80% power consumption in the balun, contributing to the noise to the LNA. This noise due to the balun is compensated by the high gain at the balun stage.

IV. Conclusions

This paper described a compact on-chip RFIC transformer balun for LNA. Both the primary and secondary are toroidal-type spreading over four metal layers. Commercially available software IE3D was used as the design tool. It was demonstrated with both simulation and experiment that the described balun structure provides very good differential amplitude and phase balance. The balun showed high power consumption due to low quality factor at primary, a result of the thin-metal aluminum in spiral windings. This drawback can be compensated by high balun voltage gain from the turn ratio and front tuning.

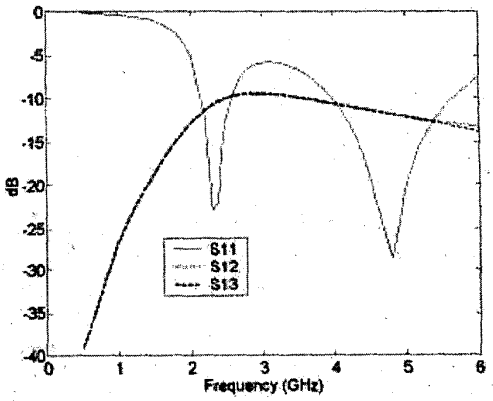

Figure 7. Return and insertion losses of the transformer balun with an LNA load and front capacitance tuning.

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